ABSTRACT OF THE DISCLOSURE

There is provided a power transistor, as well as a semiconductor integrated circuit using the power transistor, in which malfunctions of parasitic PNP transistor and circuit malfunctions due to latch-up of peripheral circuits can be prevented. In a power transistor composed of a plurality of vertical PNP transistors arrayed on a P-type silicon substrate, a singularity or plurality of electrode portions of an N^+ type buried layer formed to isolate the P-type silicon substrate and collectors of the plurality of vertical PNP transistors from each other are provided in an active region of the power transistor.